Amendment to the Claims:

This listing of the claims will replace all prior versions, and listings of claims in the present patent application:

Listing of Claims:

Claim 1 (currently amended). A programmable broadband downstream module configured to be communicatively coupled to a digital headend, comprising:

a bus interface configured to be communicatively coupled to said digital headend, said bus interface configured to receive a plurality of control data packets and a plurality of transport packets, said plurality of transport packets comprising, ~~including:~~

a plurality of video transport packets communicated asynchronously,

a plurality of transmission control protocol/internet protocol (TCP/IP) data transport packets communicated asynchronously, and

a plurality of voice transport packets communicated asynchronously;

a processor ~~programmable CPU~~ operatively coupled to said bus interface, said processor ~~programmable CPU~~ configured to combine said plurality of transport packets ~~to generate a programmable CPU output;~~ and

a programmable logic operatively coupled to said processor ~~programmable CPU~~, said programmable logic configured to generate a synchronous output for said plurality of transport packets.

Claim 2 (currently amended). The programmable broadband downstream module of claim 1, further comprising a downstream QAM modulator ~~downstream modulator~~ configured to receive and modulate said synchronous output for downstream

transmission, said downstream QAM modulator ~~downstream modulator~~ configured to generate a downstream modulator output.

Claim 3 (original). The programmable broadband downstream module of claim 2, further comprising an upconverter operatively coupled to said downstream modulator, said upconverter configured to generate a particular RF frequency output for said downstream modulator output.

Claim 4 (currently amended). The programmable broadband downstream module of claim 1, further comprising, a first memory ~~CPU memory support~~ module operatively coupled to said processor ~~programmable CPU~~, said first memory ~~CPU memory support~~ module configured to provide memory resources for said plurality of control data packets and said plurality of transport packets.

Claim 5 (currently amended). The programmable broadband downstream module of claim 4, further comprising a second memory module operatively coupled to said programmable logic, said second memory module configured to act as a buffer and store said plurality of transport packets and said plurality of control data packets.

Claim 6 (currently amended). The programmable broadband downstream module of claim 2 ~~claim 1~~ further comprising an encryption circuit operatively coupled between said programmable logic and said downstream QAM modulator ~~downstream modulator~~, said encryption circuit configured to encrypt said synchronous output.

Claim 7 (original). The programmable broadband downstream module of claim 1 wherein said plurality of transport packets are a plurality of MPEG-2 transport packets.

Claim 8 (currently amended). The programmable broadband downstream module of claim 7 wherein said processor ~~programmable CPU~~ is configured to perform bit-stuffing.

Claim 9 (currently amended). The programmable broadband downstream module of claim 8 wherein said processor ~~programmable CPU~~ is configured to provide for insertion of control data into said plurality of MPEG-2 transport packets.

Claim 10 (currently amended). The programmable broadband downstream module of claim 9 wherein said processor ~~programmable CPU~~ is configured to perform byte insertions.

Claim 11 (currently amended). A programmable broadband downstream module configured to be communicatively coupled to a digital headend, comprising:

a bus interface configured to be communicatively coupled to said digital headend, said bus interface configured to receive a plurality of control data packets and a plurality of transport packets, said plurality of transport packets comprising, ~~including:~~

a plurality of video transport packets communicated asynchronously, and

a plurality of transmission control protocol/internet protocol (TCP/IP) data transport packets communicated asynchronously;

a processor ~~programmable CPU~~ operatively coupled to said bus interface, said processor ~~programmable CPU~~ configured to combine said plurality of transport packets ~~to generate a programmable CPU output~~; and

a programmable logic operatively coupled to said processor ~~programmable CPU~~, said programmable logic configured to generate a synchronous output for said plurality of transport packets.

Claim 12 (currently amended). The programmable broadband downstream module of claim 11, further comprising a downstream QAM modulator ~~downstream modulator~~ configured to receive and modulate said synchronous output for downstream transmission, said downstream QAM modulator ~~downstream modulator~~ configured to generate a downstream modulator output.

Claim 13 (original). The programmable broadband downstream module of claim 12, further comprising an upconverter operatively coupled to said downstream modulator,

said upconverter configured to generate a particular RF frequency output for said downstream modulator output.

Claim 14 (currently amended). The programmable broadband downstream module of claim 11, further comprising, a first memory ~~CPU memory support~~ module operatively coupled to said processor ~~programmable CPU~~, said first memory ~~CPU memory support~~ module configured to provide memory resources for said plurality of control data packets and said plurality of transport packets.

Claim 15 (currently amended). The programmable broadband downstream module of claim 14, further comprising a second memory module operatively coupled to said programmable logic, said second memory module configured to act as a buffer and store said plurality of transport packets and said plurality of control data packets.

Claim 16 (currently amended). The programmable broadband downstream module of claim 12 ~~claim 11~~ further comprising an encryption circuit operatively coupled between said programmable logic and said downstream QAM modulator ~~downstream modulator~~, said encryption circuit configured to encrypt said synchronous output.

Claim 17 (original). The programmable broadband downstream module of claim 11 wherein said plurality of transport packets are a plurality of MPEG-2 transport packets.

Claim 18 (currently amended). The programmable broadband downstream module of claim 17 wherein said processor ~~programmable CPU~~ is configured to perform bit-stuffing.

Claim 19 (currently amended). The programmable broadband downstream module of claim 18 wherein said processor ~~programmable CPU~~ is configured to provide for insertion of control data into said plurality of MPEG-2 transport packets.

Claim 20 (currently amended). The programmable broadband downstream module of claim 19 wherein said processor ~~programmable CPU~~ is configured to perform byte insertions.

Claim 21 (currently amended). A programmable broadband downstream module configured to be communicatively coupled to a digital headend, comprising:

a bus interface configured to be communicatively coupled to said digital headend, said bus interface configured to receive a plurality of control data packets and a plurality of transport packets, said plurality of transport packets comprising, ~~including:~~

a plurality of video transport packets communicated asynchronously, and

a plurality of voice transport packets communicated asynchronously;

a processor ~~programmable CPU~~ operatively coupled to said bus interface, said processor ~~programmable CPU~~ configured to combine said plurality of transport packets ~~to generate a programmable CPU output~~; and

a programmable logic operatively coupled to said processor ~~programmable CPU~~, said programmable logic configured to generate a synchronous output for said plurality of transport packets.

Claim 22 (currently amended). The programmable broadband downstream module of claim 21, further comprising a downstream QAM modulator ~~downstream modulator~~ configured to receive and modulate said synchronous output for downstream transmission, said downstream QAM modulator ~~downstream modulator~~ configured to generate a downstream modulator output.

Claim 23 (original). The programmable broadband downstream module of claim 22, further comprising an upconverter operatively coupled to said downstream modulator, said upconverter configured to generate a particular RF frequency output for said downstream modulator output.

Claim 24 (currently amended). The programmable broadband downstream module of claim 21, further comprising, a first memory ~~CPU memory support~~ module operatively coupled to said processor ~~programmable CPU~~, said first memory ~~CPU memory support~~ module configured to provide memory resources for said plurality of control data packets and said plurality of transport packets.

Claim 25 (currently amended). The programmable broadband downstream module of claim 24, further comprising a second memory module operatively coupled to said programmable logic, said second memory module configured to act as a buffer and store said plurality of transport packets and said plurality of control data packets.

Claim 26 (currently amended). The programmable broadband downstream module of claim 22 ~~claim 21~~ further comprising an encryption circuit operatively coupled between said programmable logic and said downstream QAM modulator ~~downstream modulator~~, said encryption circuit configured to encrypt said synchronous output.

Claim 27 (original). The programmable broadband downstream module of claim 21 wherein said plurality of transport packets are a plurality of MPEG-2 transport packets.

Claim 28 (currently amended). The programmable broadband downstream module of claim 27 wherein said processor ~~programmable CPU~~ is configured to perform bit-stuffing.

Claim 29 (currently amended). The programmable broadband downstream module of claim 28 wherein said processor ~~programmable CPU~~ is configured to provide for insertion of control data into said plurality of MPEG-2 transport packets.

Claim 30 (currently amended). The programmable broadband downstream module of claim 29 wherein said processor ~~programmable CPU~~ is configured to perform byte insertions.

Claim 31 (currently amended). A programmable broadband downstream module configured to be communicatively coupled to a digital headend, comprising:

a bus interface configured to be communicatively coupled to said digital headend, said bus interface configured to receive a plurality of control data packets and a plurality of transport packets, said plurality of transport packets comprising, ~~including:~~

a plurality of transmission control protocol/internet protocol (TCP/IP) data transport packets communicated asynchronously, and

a plurality of voice transport packets communicated asynchronously;

a processor ~~programmable CPU~~ operatively coupled to said bus interface, said processor ~~programmable CPU~~ configured to combine said plurality of transport packets ~~to generate a programmable CPU output~~; and

a programmable logic operatively coupled to said processor ~~programmable CPU~~, said programmable logic configured to generate a synchronous output for said plurality of transport packets.

Claim 32 (currently amended). The programmable broadband downstream module of claim 31, further comprising a downstream QAM modulator ~~downstream modulator~~ configured to receive and modulate said synchronous output for downstream transmission, said downstream QAM modulator ~~downstream modulator~~ configured to generate a downstream modulator output.

Claim 33 (original). The programmable broadband downstream module of claim 32, further comprising an upconverter operatively coupled to said downstream modulator,

said upconverter configured to generate a particular RF frequency output for said downstream modulator output.

Claim 34 (currently amended). The programmable broadband downstream module of claim 31, further comprising, a first memory ~~CPU memory support~~ module operatively coupled to said processor ~~programmable CPU~~, said first memory ~~CPU memory support~~ module configured to provide memory resources for said plurality of control data packets and said plurality of transport packets.

Claim 35 (currently amended). The programmable broadband downstream module of claim 34, further comprising a second memory module operatively coupled to said programmable logic, said second memory module configured to act as a buffer and store said plurality of transport packets and said plurality of control data packets.

Claim 36 (currently amended). The programmable broadband downstream module of claim 32 ~~claim 31~~ further comprising an encryption circuit operatively coupled between said programmable logic and said downstream QAM modulator ~~downstream modulator~~, said encryption circuit configured to encrypt said synchronous output.

Claim 37 (original). The programmable broadband downstream module of claim 31 wherein said plurality of transport packets are a plurality of MPEG-2 transport packets.

Claim 38 (currently amended). The programmable broadband downstream module of claim 37 wherein said processor ~~programmable CPU~~ is configured to perform bit-stuffing.

Claim 39 (currently amended). The programmable broadband downstream module of claim 38 wherein said processor ~~programmable CPU~~ is configured to provide for insertion of control data into said plurality of MPEG-2 transport packets.

Claim 40 (currently amended). The programmable broadband downstream module of claim 39 wherein said processor ~~programmable CPU~~ is configured to perform byte insertions.